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Energy Efficient Multiplier Design Using Gdi Logic

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Abstract: *Addition and multiplications are a fundamental blocks to perform all operations in digital circuits. A high performance multiplier is a one of the key component in designing applications of integrated circuits. In designing integrated circuits power is a one of premium resources a designer tries to save when designing the circuit or system.The major issue for design of adderpower dissipation, delay. These issues can be overcome by new technique GATE DIFFUSION INPUT (GDI) logic technique which is commonly occurring a threshold voltage problem, so it does not allow adders without additional inverters. In this paper three full adders designed with full swing gates by using GDI logic called as proposed designs. The proposed designs are improve in their circuit performance. Performance of proposed designs having a low power consumption when compared all other designs in simulation results. The goal is to proposed full adders extended with multiplier to reduce the complexity of design as well as make a low energy consumption and high speed in designing systems.*
Keywords*: Adder, GDI logic,Digital design, Full swing.*

I. Introduction

Due to rapid development of portable applications, electronics market is becoming more competitive, which results in consumer electronic products requiring even more stringently high quality. Therefore, the integrated circuit (IC) designers have to consider more important issues such as chip area, power consumption, operation speed, circuit regularity, and so on [15].In most of the digital circuits, adders performs a major role which influences the overall system performance. Addition is a fundamental block to perform any operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) and microprocessors architectures[4].Power consumption and speed would be the othertwo important criteria when it comes to the design of full adders. The design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. Therefore, power delay product or energy consumption per operation has been introduced to accomplish optimal design trade-offs. The performance of digital circuits can be optimized by proper selection of logic styles.In this paper we are designed low power consumption adders extended with multiplier to reduce the complexity and reduce the power consumption when compared with other designs. This may reduce overall capacitances which in turn will increase the speed and decrease the power dissipation. The adder design implemented using transmission gate with a new technique GDI (Gate Diffusion Input) . This technique allows reducing power consumption, delay and area of a low power digital circuits, while maintaining low complexity of logic design[12].

II. Gdi Logic

Gate diffusion input (GDI) - a new technique of low-power digital combinatorial circuit design is described. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various pass-transistor logic design techniques is presented. The different methods are compared with respect to the layout area, number of devices, delay, and power dissipation. Issues like technology compatibility, top-down design, and precomputing synthesis are discussed, showing advantages and drawbacks of GDI compared to other methods. Several logic circuits have been implemented in various design styles. Their properties are discussed, simulation results are reported, and measurements of a test chip are presented.Basic GDI logic input as shown in figure.

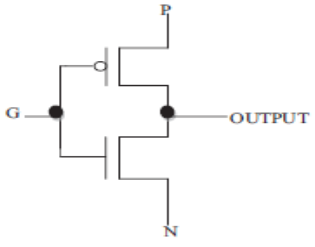

FIGURE 1:-GDI CELL

At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.1) The GDI cell contains three inputs:G(common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.
Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method. In this paper, most of the designed circuits were based on the F1 and F2 functions. The reasons for this are as follows.
1) Both F1 and F2 are complete logic families (allows realization of any possible two-input logic function).
2) F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased.
3) When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOSbulks to Out are directly polarized and there is a shortbetween N and P, resulting in static power dissipation and $V_{OUT\sim} 0.5\ V_{DD}$.

PROPOSED ADDER IN GDI:-
Three proposed full adder designs featured with GDI full swing gates with the goal to minimize the circuit complexity and to achieve speed at cascaded operation. The strategy is to avoid threshold voltage losses with the help of full swing gatesswing gates.

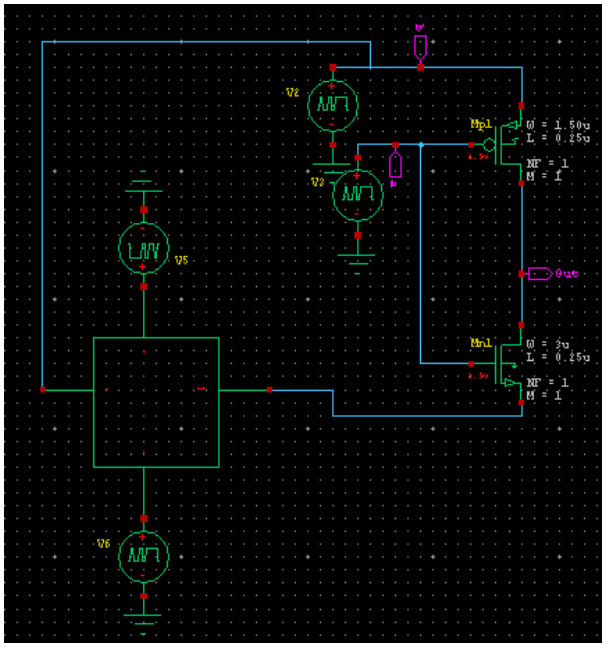

FIGURE 2:-Xor gate

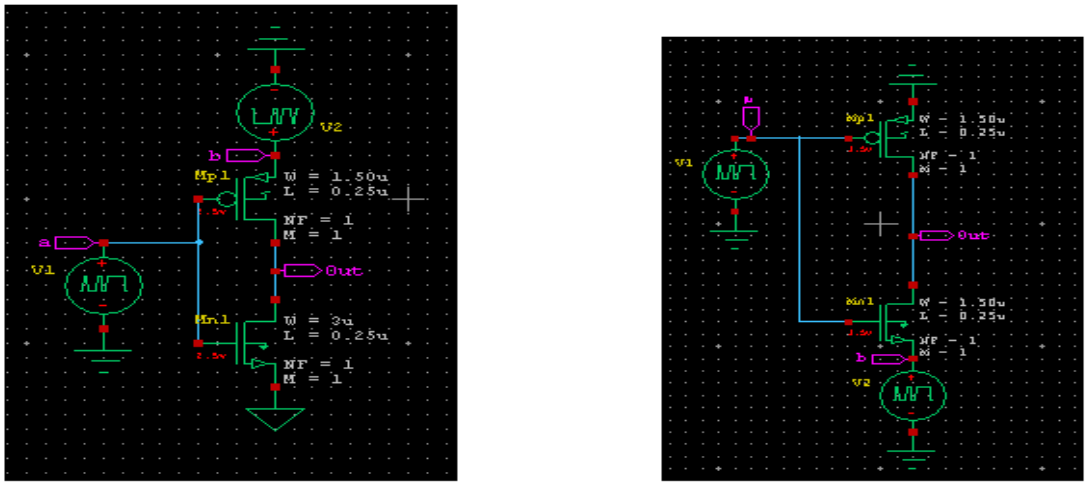

FIGURE 3:-Or gate

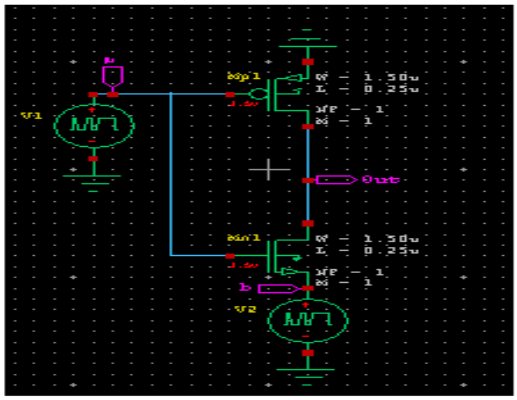

FIGURE 4:-And gate

The logic function of full adder can be
represented as below equations
Sum= A XOR B XOR Cin (1)
Cout= A AND B + B AND Cin+ A AND Cin (2)
From above equations three basic gates are needed for implementing the function i.e., AND, OR and XOR with their transistor level diagrams. The operational characteristics of these gates are given table. The output voltages are degraded by threshold voltage drop for certain input combinations. The reduction in output voltage increases significantly withincrease in the number of stages.

FULL ADDER DESIGNS:-
The full adders are design of GDI logic with the help of full swing gates using AND, OR, XOR. This design completely eliminates the full swing restoration buffers that results in improve in their performance. Three designs are rewrite by the full adder expressions as listed below

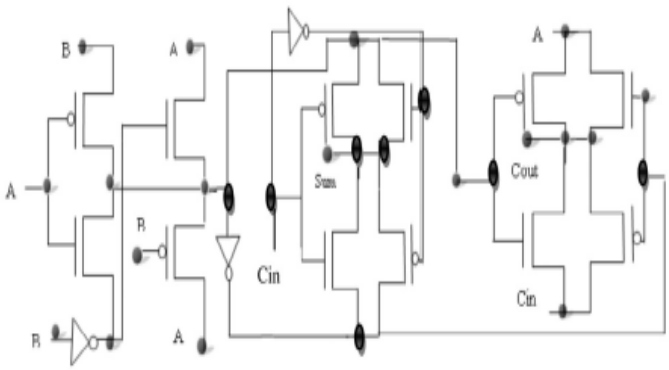

FIGURE 5:-Design1

Design1 Full adder having a output expressions for Sum and Cout with respective below equations 3,4
Sum=Cin(A XOR B) +Cin(A XNORB) (3)
Cout= (A XOR B)Cin+ (A XOR B)A (4)
Design 1 uses XOR output as an intermediate result for computing *Sum* and Cout. *Sum* output can be attained by multiplexing the XOR and its inverted version XNOR through *Cin*input. The *Cout*is obtained by multiplexing the inputs *A* and *Cin*whose output is controlled by the selection input, i.e. XOR output of *A* and *B* inputs. The presence of inverter on the critical path increases the delay of the whole circuit. This design is simple and requires a total of 18transistors for realizing the full adder function.
Design 2 Full adder having a output expressions for sum and cout but there is a difference in design. This design of full adder consists of XOR, AND, OR Gates when compared to previous design.
Sum= A XOR B XOR Cin(5)
Cout= Cin(A AND B) +Cin(A OR B) (6)

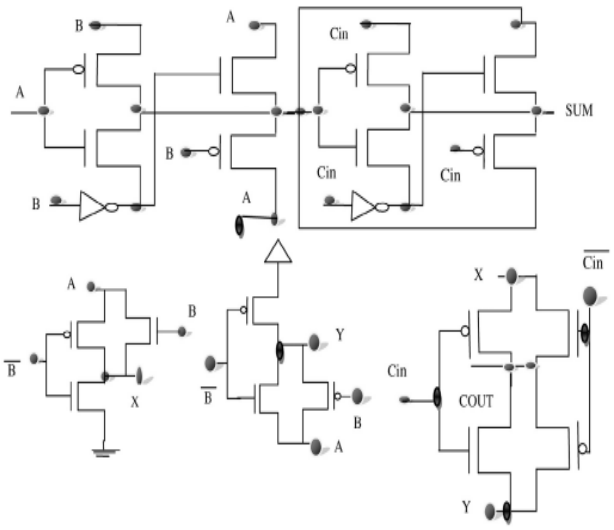

FIGURE 6:-Design 2

Design 2 based full adder. AND and OR gates are designed based on F1 and F2, respectively. Multiplexing the AND andOR operation through Carry input *Cin*helps in *Cout*realization.The XOR operation on the inputs *A*, *B* and *Cin*achieves *Sum* function.

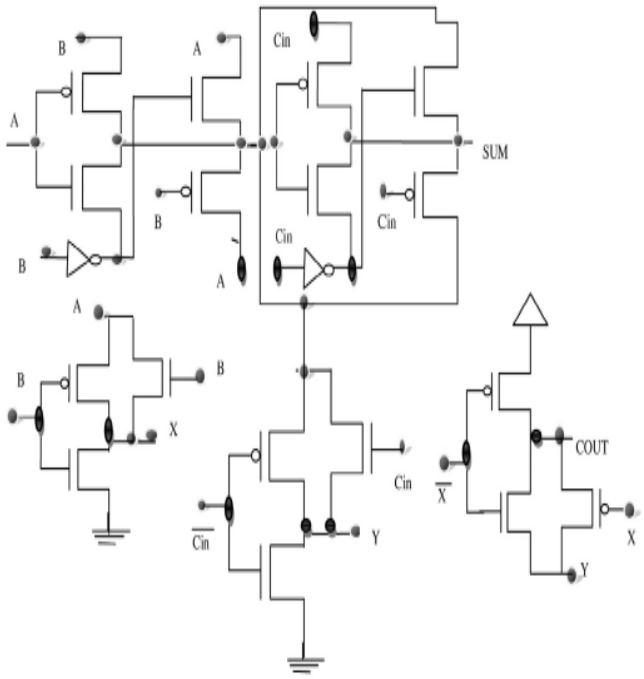

FIGURE 7:-Design 3

Design 3 Full adder having a output expressions for sum and cout with respective equations 7, 8

Sum= A XOR B XOR Cin(7)

Cout= A AND B + (A XOR B)Cin(8)

Design 3uses XOR module that plays an important role since *Sum* output can be achieved by XORing the inputs *A*, *B* and *Cin*. The output*C*outis obtained with the help of AND and OR followed by XOR gate.The realization of AND and OR gate can be done with the help offull swing F1 and F2 gates. The GDI based F1 and F2 enables the implementation of AND and OR with only 3 transistors where as CMOS needs 6 transistors for achieving the same. The intermediate XOR gate output is used for computing *Cout*output.

CMOS FULL ADDER DESIGN:-

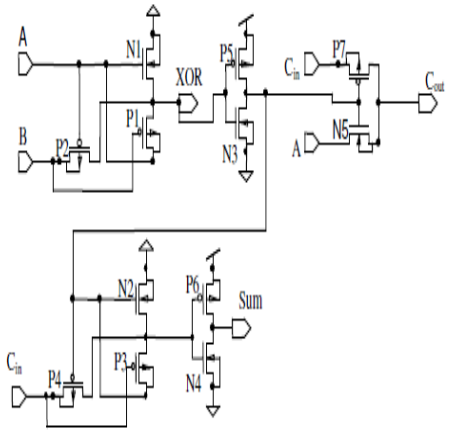

FIGURE 8:- Design4

In this design Cout (carry out) signal has been generated by two transistor multiplexer block with Cin, A and XNOR signal. Sum signal is generated with XNOR signal generated by inverter and Cin signal. This circuit contains 12 transistors with xor gates.As CMOSinverter is responsible for major portion of power consumption in this adder circuit.
These designs are extended with multipliers for low energy consumption.

MULTIPLIERS:-

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. To achieve speed improvements Wallace Tree algorithm can be used to reduce the number of sequential adding stages. Further by combining both Modified Booth algorithm and Wallace Tree technique we can see advantage of both algorithms in one multiplier. However with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing. On the other hand "serial-parallel" multipliers compromise speed to achieve better performance for area and power consumption. The selection of a parallel or serial multiplier actually depends on the nature of application. In this lecture we introduce the multiplication algorithms and architecture and compare them in terms of speed, area, power and combination of these metrics. Based on full adder designs 3*3 multipliers are designed.

3*3MULTIPLIER:-

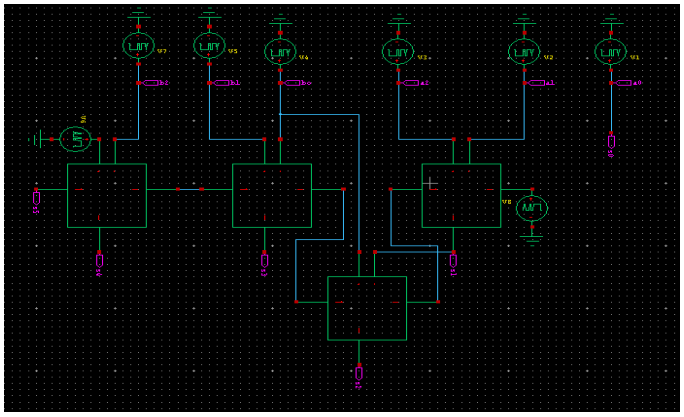

FIGURE 9:- 3*3 Multiplier

SIMULATION RESULTS FOR MULTIPLIERS:-

For simulation environment Full adders based on other logic are taken for comparison with the proposed designs.In addition to these adders based on XOR gate are also taken into account. It has a full voltage swing and buffered *Sum* and *Cout*signals. It uses the feedback transistors for providing full swing. The design which uses the combination of CMOS and PTL to generate *Sum* and *Cout*,respectively is called hybrid design. It uses 24 transistors in this regard, which lies between CMOS and transmission gate. It is very clear that CPL logic consumes relatively more power due to more number of transistors required for its design. In the case of hybrid design, this equally performs well with CMOS in terms of delay and power consumption. However, it takes reduced number of transistor count compared to CMOS for its design. Whereas the Three proposed GDI based full adders, especially *Design 2* outperforms all the other adders in both delay and Energy Delay Product (EDP). This would have resulted due to reduced transistor count on the paths between input and output. This will also lead to the decrease in the parasitic capacitance at the *Sum* and *Cout*nodes.The performance metrics of all the simulated adders such as delay, power consumption, energy consumption and process variation analysis are discussed.Three proposed full adder designs have advantages and also limitations. *Design 1* is an optimal candidate for the applications in which minimum transistor count and low power is a design requirement. The *Design 2* provides lower EDP and minimum delay, so it can be suitable for battery operated and real-time applications. It has slightly increased in transistor count compared with Design 1. Design 3 lies midway between Design 1 and Design 2, and offers lowerdelay than Design 1 as shown in results from given table

TABLE 1

Logic	Power (uw)	Delay (ns)	Transistors
Design1	3.26	15.49	18
Design2	107.36	0.164	22
Design3	32.49	19.86	23

From the obtained results, it can be concludedthat all three designs operate with less energy consumptionthan existing adders taken for comparison. Hence these design can be extended with multiplier to reduce the complexity to make an low energy consumption circuits in system design. Multiplier power analysis as shown in table.

TABLE 2

Design	Power (uw)	Delay (ns)	PDP
3*3 Multiplier using Design1	146.43	0.313	0.045
3*3 Multiplier using Design2	4114.66	19.97	82.16
3*3 Multiplier using Design3	451.27	19.73	8.903
3*3 Multiplier using cmos	0.130	19.90	2.587

III. Conclusion

In this paper 3*3 multiplier is proposed based on GDI full adder designs. Out of the three designs based multipliers design1 is superior than other two designs. Comparing with cmos based multiplier and design2, design3 based multipliers, design1 based multiplier has less delay. The power delay product of design1 is 0.045.

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